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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/825,377	04/02/2001	Yi Hu	KELLY-4	1648

7590 05/25/2004

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EXAMINER	
LERNER, MARTIN	

ART UNIT	PAPER NUMBER
2654	

DATE MAILED: 05/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/825,377	Applicant(s) HU ET AL.	
	Examiner Martin Lerner	Art Unit 2654	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 4 to 6, 10 to 18, and 20 to 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4 to 6, 10 to 18, and 20 to 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 4 to 6, 10, 15 to 17, 20, and 24 to 25 are rejected under 35 U.S.C. 102(e) as being anticipated by *Nguyen et al. ('054)*.

Regarding independent claims 1 and 24, *Nguyen et al. ('054)* discloses a codec (column 4, line 10) processor and computer program product, comprising:

"a programmed digital signal processor and an accelerator core in which computation of a coding algorithm is divided between the digital signal processor and the accelerator core" – bitstream processor 245 ("a programmed digital signal processor") is a fixed hardware processor which performs specific functions on an input or output bitstream as variable length (Huffman) coding and decoding (column 9, lines 5 to 17: Figure 2); multimedia processor 110 includes a processing core 200 which contains a general purpose processor 210 and a vector processor 220 ("an accelerator core") (column 5, lines 46 to 56: Figure 2); the vector processor is designed to perform

computationally intensive tasks requiring manipulation of large data blocks, while the general purpose processor acts as the master processor to the vector processor (column 3, lines 54 to 58);

"wherein the accelerator core includes a vector processor capable of processing multiple items of data simultaneously, said vector processor comprising a plurality of similar operational units capable of carrying out simultaneous data processing operations" – the term vector processor refers to a processor which executes instructions having vector operands, i.e. operands each containing multiple data elements of the same type (column 5, lines 50 to 54: Figure 2); vector processor 220 consists of a pipelined RISC central processing unit and has a plurality of vector registers; each vector register can contain up to 32 data elements ("a plurality of similar operational units carrying out simultaneous data processing operations") (column 6, lines 7 to 35); additionally, *Nguyen et al. ('054)* discloses vector processor 220 has SIMD (single-instruction multiple-data) architecture (column 6, lines 7 to 10); SIMD is a set of operations for efficiently handling large quantities of data in parallel in a vector processor (*Wikipedia*);

"said vector processor being operative to execute program instructions whereby a data processing operation is assigned for performance by one or more of the operational units on a plurality of data elements" – instruction cache 292 and data cache 294 are for use with vector processor 220; ROM cache 270 contains frequently used instructions and data for vector processor 220 (column 9, lines 34 to 61: Figure 4).

Regarding claim 4, *Nguyen et al. ('054)* discloses vector processor 220 has SIMD (single-instruction multiple-data) architecture (column 6, lines 7 to 10).

Regarding claims 5 and 6, *Nguyen et al. ('054)* discloses vector processor 220 performs signal processing for G.728 and G.723 (column 6, lines 53 to 61); G.728 and G.723 are speech coding standards to perform CELP coding of speech.

Regarding claim 10, *Nguyen et al. ('054)* discloses vector processor 220 has a vector register file with a plurality of vector registers for performing vector and scalar operations (column 6, lines 7 to 36).

Regarding claims 15 to 17, *Nguyen et al. ('054)* discloses SRAM block 260 is divided into four memory banks to form instruction cache 292 and data cache 294 for use with vector processor 220; ROM cache 270 contains frequently used instructions and data for vector processor 220; data pipeline 410 performs the data switchboard function to create multiple simultaneous data communication paths between vector processor 220 and SRAM block 260; thus, vector processor 220 shares common RAM and ROM memory units (column 9, lines 34 to 50: Figure 4).

Regarding claim 20, *Nguyen et al. ('054)* discloses micro-instructions ("microcode") (column 11, line 66).

Regarding claim 25, it is implicit that hardware definition language is the design tool for microprocessors; moreover, this is a process limitation in a claim to a computer program product, not deserving of patentable weight. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP 2113.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11 to 14, 18, and 21 to 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Nguyen et al. ('054)* in view of *Nguyen et al. ('194)*.

Regarding claims 11 to 14, *Nguyen et al. ('054)* discloses that vector processor 220 has a plurality of registers, and a vector can span two registers, but does not set forth specifics about whether operational units can perform operations upon the output of one or more of the operational units, whether each operational unit can store the result of an operation in the register bank, whether an operation can be performed on the output of an operational unit to derive a further output, or whether outputs from a plurality of operational units can be summed.

However, *Nguyen et al. ('194)* provides specifics on a vector processor 100 having eight execution units. (Column 4, Lines 20 to 35: Figure 1) Instructions performed by vector processor 100 include inter-element arithmetic ("each operational unit can perform operations upon the output of one or more of the operational units"), can store results in accumulator 540 ("each operational unit can store the result of an operation in the register bank"), perform multi-cycle arithmetic instructions ("an

operation can be performed on the outputs of a plurality of the operational units to derive a further output value"), where arithmetic instructions involving summing and averaging ("the outputs of a plurality of the operational units can be summed") (column 5, lines 39 to 58: Figure 6: Table A.4). *Nguyen et al. ('194)* also states that more complex instructions can be performed by chaining together and sharing functional units. (Column 4, Lines 63 to 67: Figure 4) It is suggested that dividing the input data stream into smaller data slices allows processing in less time, and that because many operations can share the functional units, the integrated circuit is less expensive and smaller. (Column 1, Lines 44 to 56; Column 3, Lines 29 to 45) It would have been obvious to one having ordinary skill in the art to perform the operations taught by *Nguyen et al. ('194)* in the vector processor of *Nguyen et al. ('054)* for the purpose of processing in less time and with a less expensive integrated circuit.

Regarding claim 18, *Nguyen et al. ('194)* teaches vector processor has functional units performing multiply-and-accumulate (MAC) operations (column 1, lines 57 to column 2, line 3; column 4, lines 36 to 62: Figure 4).

Regarding claims 21 to 23, *Nguyen et al. ('194)* teaches a data path slice 410 can include a Booth decoder as a multiplier (column 5, lines 1 to 24); a multiplier is a finite state machine, and a Booth decoder is programmable and includes memory.

Response to Arguments

5. Applicants' arguments with have been considered but are moot in view of the new grounds of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to Applicants' disclosure.

Fung, Jennings, III, Lee et al., and Raz et al. disclose related art.

Wikipedia discloses that SIMD is a set of operations for efficiently handling large quantities of data in parallel in a vector processor.

Kleine discloses an exemplary Booth decoder.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Martin Lerner whose telephone number is (703) 308-9064. The examiner can normally be reached on 8:30 AM to 6:00 PM Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richemond Dorvil can be reached on (703) 305-9645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ML
4/21/04

Martin Lerner
Examiner
Group Art Unit 2654